

### **Amendments to the Drawings**

The Examiner objected to **Figs. 8A, 8B, and 8C** for lacking labels consistent with the specification. Applicants request clarification of the Examiner's objection. Specifically, Applicants assert that **Figures 8A, 8B, and 8C** are consistent with the specification, in that the figures show an asynchronous transfer list 800, a USB host controller internal state 802, and a queue head 804 as described in the specification. Applicants further assert that these figures are sufficient to illustrate the description given in the specification.

## REMARKS/ARGUMENTS

The following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

### 35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1, 11, 21, and 27 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,763,391 to Ludtke ("Ludtke").

Claim includes a limitation of reclaiming resources assigned to a work item whenever a coherency signal is generated. Ludtke does not disclose such a limitation, and as a result does not anticipate claim 1. Specifically, Ludtke discloses a tagging mechanism to tag selections and ensure that a service will continue to be delivered until it is requested that the service be removed (Col. 9, lines 16-24). This mechanism uses a scope bit to determine the extent of the selections to be cleared (Col. 9, lines 35-60). When a command to clear a selection is issued, the sourcing device clears the command if the scope bit is set to zero. However, the sourcing device only clears the command, and does not reclaim resources assigned to a work item, as in claim 1. As a result, Ludtke does not anticipate claim 1.

Examiner rejected claims 1, 10, 11, 20, 21, and 27 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,205,501 to Brief, et al. ("Brief").

Claim 1 includes a limitation of generating a coherency signal independent of a work item utilizing an expansion bus host controller in response to removing the work item. Brief does not disclose such a limitation, and therefore does not anticipate claim 1. Specifically, Brief discloses a control word pointer (CWP) that points to a control word which includes several bits that describe the state of a buffer (Col. 8, line 59-Col. 9, line 32). The buffer can be reclaimed when certain bits of the control word indicate that the buffer state is complete. However, the control word pointer is associated with the control word, which indicates that the buffer may be reclaimed. As a result, Brief does not disclose generating a coherency signal independent of a work item, and Brief does not anticipate claim 1.

Examiner rejected claims 1, 5 – 10, 11, 15 – 20, 21, and 23 – 30 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,804,762 to Dussud, et al. (“Du ssud”).

Claim 1 includes a limitation of generating a coherency signal independent of a work item utilizing an expansion bus host controller in response to removing the work item. Dussud does not disclose such a limitation, and as a result does not anticipate claim 1. Specifically, Dussud discloses a write barrier system that determines whether a pointer exists in an ephemeral range (Col. 8, line 58 –Col. 9, line 7). If the pointer exists in the ephemeral range, the pointer is referred to the garbage collection system. This system only determines that a pointer is outside of a predetermined range. Dussud does not disclose a system where a work item may be removed. Further, Dussud does not disclose that a coherency signal is generated, since when the pointer is found to be

outside of the limits (i.e., ephemeral), the pointer is sent to garbage collection. As a result, claim 1 is not anticipated by Dussud.

Independent claims 11, 21, and 27 include limitations similar to those discussed above regarding claim 1. As a result, since claim 1 is not anticipated by Ludkte, Brief, or Dussud, claims 11, 21, and 27 are also not anticipated by Ludkte, Brief, or Dussud. Furthermore, the remaining claims depend from one of the independent claims discussed above and therefore also include the distinguishing claim limitations. As a result, the remaining claims are also not anticipated and are patentable.

#### 35 U.S.C. § 103(a) Rejections

Examiner rejected claims 2-4, 12 - 14 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Ludtke in view of Universal Host Controller Interface (UHCI) Design Guide, Revision 1.1 by Intel ("Intel").

Examiner rejected claims 2 – 4, 12 – 14 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Brief in view of Intel.

Examiner rejected claims 2 – 4, 12 – 14 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Dussud in view of Intel.]

Intel does not disclose the limitations discussed above regarding the independent claims. Since the independent claims are not anticipated by Ludkte, Brief, or Dussud, claims 2-4, 12-14, and 22 are patentable over Ludkte, Brief, or Dussud in view of Intel.

## CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen Hartounian at (408) 720-8300, x352.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: May 12, 2005



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Arlen M. Hartounian  
Reg. No. 52,997

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025-1026  
(408) 720-8300